CLAIMS

What is claimed is:

1. A method to conserve power comprising:

in a digital signal processor integrated circuit including an internal memory, a reduced instruction set computing (RISC) processor and one or more digital signal processing (DSP) units,

selectively swapping activity between the RISC processor and the one or more DSP units;

selectively stopping the clocking of respective one or more DSP units; and

selectively activating one of a plurality of memory clusters in the internal memory and maintaining a state of all other memory clusters.

2. The method of claim 1, wherein

the selective swapping activity between the RISC processor and the one or more DSP units includes

activating and inactivating bus drivers on data paths in the RISC processor and the one or more DSP units.

3. The method of claim 1, wherein

selectively activating one of a plurality of memory clusters in the internal memory and maintaining a state of all other memory clusters includes

selecting a data flow path between the activated memory cluster and the RISC processor and the one or more DSP units to change state while maintaining the state on data flow paths between the inactivated memory clusters and the RISC processor and the one or more DSP units.

4. The method of claim 1, wherein the selective stopping the clocking of respective one or more DSP units is responsive to those one or more DSP units being inactive.

5. The method of claim 1, wherein the selective stopping the clocking of respective one or more DSP units is responsive to those one or more DSP units not executing an instruction.

6. The method of claim 1, wherein the selective activating one of the plurality of memory clusters in the internal memory is responsive to addressing a memory location within the respective one of the plurality of memory clusters.

7. A method to conserve power in an integrated circuit comprising:

providing a bus multiplexer between a memory storing operands and a functional unit of the integrated circuit, the bus multiplexer and the memory coupled to a global bus having a first bit width, the bus multiplexer to receive data from the memory on the global bus; and

selectively multiplexing the data on the global bus of the first bit width onto a first local bus in the functional unit, the first local bus having a second bit width less than the first bit width.

8. The method of claim 7, wherein

the second bit width of the first local bus is less than the first bit width of the global bus to lower the switching capacitance.

9. The method of claim 7, wherein
the routing length of the first local bus is greater than the routing length of the global bus.

10. The method of claim 7, further comprising:
selectively multiplexing the data on the global bus of the first bit width onto a second local bus in the functional unit, the second local bus having a third bit width less than the first bit width and the second bit width.

11. The method of claim 10, wherein
the second bit width of the first local bus and the third bit width of the second local bus is less than the first bit width of the global bus to lower the switching capacitance.

12. The method of claim 10, wherein
the routing length of the first local bus and the second local bus is greater than the routing length of the global bus.

13. The method of claim 7, wherein
the memory is a local data memory and the functional unit is a digital signal processing unit.

14. A method of laying out an integrated circuit to lower power consumption, the method comprising:

routing a first bus over a first length coupled between a data memory and a plurality of functional units, the first bus having a first bit width; and

providing each of the plurality of functional units coupled to the first bus including

a bus multiplexer to couple to the first bus and

routing a second bus coupled to the bus multiplexer within the functional unit over a second length, the second bus having a second bit width.

15. The method of claim 14, wherein the second bit width of the second bus is less than the first bit width of the first bus to lower the switching capacitance.

16. The method of claim 14, wherein the first length of the first bus is less than the second length of the second bus.

17. The method of claim 14, wherein

the providing each of the plurality of functional units coupled to the first bus further including

routing a third bus coupled to the bus multiplexer within the functional unit over a third length, the third bus having a third bit width.

18. The method of claim 17, wherein the third bit width of the third bus and the second bit width of the second bus are less than the first bit width of the first bus to lower the switching capacitance.

19. The method of claim 17, wherein

the first length of the first bus is less than the second length of the second bus and the third length of the third bus.

20. A bus state keeper comprising:

a plurality of multiplexers each having a select input, a first input, a second input, and an output, the output coupled to each respective bit of a first bus to keep in a steady state when inactive, the first input coupled to each respective bit of a second bus, the select input of each of the plurality of multiplexers coupled to a select signal; and

a plurality of flip flops each having a data input, a data output and a clock input, the data input coupled to each respective bit of the first bus, the data output coupled respectively to the second input of the plurality of multiplexers, the clock input coupled to a clock signal, the plurality of flip flops to store a state of the first bus.

21. The bus state keeper of claim 20, wherein,

the plurality of flip flops are clocked by the clock signal to store a state of the first bus.

22. The bus state keeper of claim 20, wherein,

the select signal input to each select input of the plurality of multiplexers selects between outputting from the plurality of multiplexers a stored state in the flip flops onto the first bus or outputting the state of the second bus onto the first bus.

23. The bus state keeper of claim 20, wherein,

the select signal input to each select input of the plurality of multiplexers selects to output from the plurality of multiplexers a stored state in the flip flops onto the first bus. to maintain a state of the first bus and conserve power.

24. The bus state keeper of claim 23, wherein,
the select signal maintains a state of the first bus to conserve power.

25. A memory in an integrated circuit to conserve power comprising:
a plurality of memory clusters, each of the plurality of memory clusters including
one or more memory blocks to store data, and
an output multiplexer; and
a memory controller to receive addresses to the memory and control the flow of data into and out of the memory; and
a plurality of buses and control lines coupled between the plurality of memory clusters and the memory controller to propagate address and data there-between and to control the activity of the plurality of memory clusters.

26. The memory of claim 25, wherein
one of the control lines between the memory controller and the plurality of memory clusters is active to activate one of the plurality of memory clusters while others are inactive to conserve power.

27. The memory of claim 25, wherein
each output multiplexer of each memory cluster couples to one of the plurality of buses between the plurality of memory clusters and the memory controller to output data

from one of the one or more memory blocks out of the memory, the output multiplexer includes

a bus multiplexer having inputs coupled to the one or more memory blocks of the memory cluster to receive data and an output, and

a bus state keeper coupled to the output of the bus multiplexer and the one of the plurality of buses between the plurality of memory clusters and the memory controller.

28. The memory of claim 27, wherein

one of the control lines between the memory controller and the one of the plurality of memory clusters is inactive to conserve power and the bus state keeper maintains the state of the one of the plurality of buses between the plurality of memory clusters and the memory controller.

29. The memory of claim 25, wherein

the memory controller includes a plurality of bus state keepers coupled to some of the plurality of buses between the plurality of memory clusters and the memory controller.

30. The memory of claim 29, wherein

one of the control lines between the memory controller and the one of the plurality of memory clusters is inactive to conserve power and the plurality of bus state keepers coupled to some of the plurality of buses between the plurality of memory clusters and the memory controller maintain the state of the some of the plurality of buses.

31. The memory of claim 25, wherein

one of the memory clusters is activated by one of the control lines while other memory clusters are deactivated by the other ones of the control lines to conserve power.

32. An integrated circuit comprising:

a RISC controller to execute RISC instructions;

one or more DSP units to execute DSP instructions; and

a unified instruction pipeline coupled to the RISC controller and the one or more DSP units, the unified instruction pipeline to decode and initiate execution of the RISC instructions and the DSP instructions of a unified RISC and DSP instruction set.

33. The integrated circuit of claim 32, wherein

the unified instruction pipeline reduces decode circuitry to conserve power otherwise needed to process RISC instructions and DSP instructions.

34. The integrated circuit of claim 32, wherein unified instruction pipeline includes

a loop buffer to store instructions in a program loop and to decode and initiate execution of the instructions stored therein while in the program loop.

35. The integrated circuit of claim 34, wherein

the loop buffer avoids continuous fetching of the instructions in the program loop from memory to conserve power.

36. A method of conserving power in an integrated circuit comprising:

selectively activating only those buses within the integrated circuit that need to transfer data;

selectively activating only those bits within active buses that need to change state; and

maintaining the state of inactive buses.

37. The method of claim 36 wherein,
the maintaining of the state of the inactive buses is performed by a bus state keeper.

38. The method of claim 36 further comprising:
maintaining the state of bits within active buses that need not change state.

39. The method of claim 38 wherein
the maintaining of the state of bits within active buses that need not change state is responsive to the type of data being transferred.